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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,817	09/22/2003	David Zimmerman	42P16614	1962

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EXAMINER	
LAU, TUNG S	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 10/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,817	ZIMMERMAN ET AL.	
	Examiner	Art Unit	
	Tung S. Lau	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/11/2005 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 5-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Nejedlo (U.S. Patent Application Publication 2004/0186688).

Regarding claim 5:

Nejedlo discloses a memory integrated circuit (IC) module, comprising: a carrier substrate (abstract, fig. 2, unit 224, 232); a plurality of first and second signal connection points installed on the substrate (fig. 2, unit 243); a plurality of memory devices installed on the substrate (fig. 2, unit 246), each of which has a

separate memory core array and separate address decoder logic (fig. 2, unit 224);

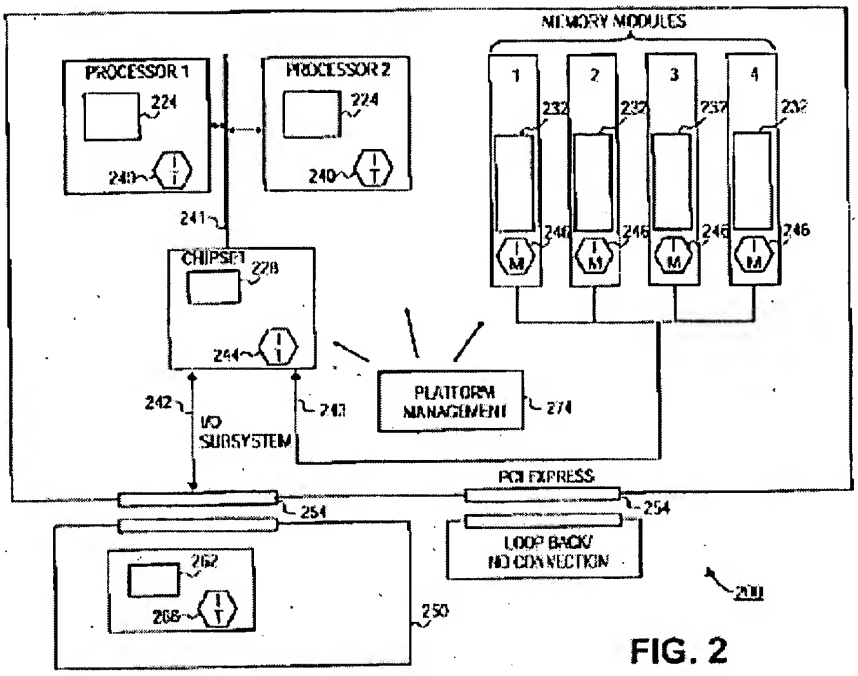


FIG. 2

and a memory buffer installed on the substrate and communicatively coupled between the plurality of first and second signal connection points and the plurality of memory devices (fig. 2, unit 228)), the buffer having a plurality of driver circuits whose outputs are coupled to the plurality of first signal connection points (fig. 2, unit 228)), respectively, and logic to a) forward read data, provided by the plurality of memory devices (fig. 2, unit 242, 243), at speed using the plurality of drivers in a normal mode of operation for the module (fig. 5, unit 602-610) and b) determine error in test symbols received from outside the module at speed using the plurality of second signal connection points in a test mode of operation for the

module during which a chip-to-chip connection between the module and another device is tested (page 3, section 0025, fig. 2, unit 224, 232, 228, 250).

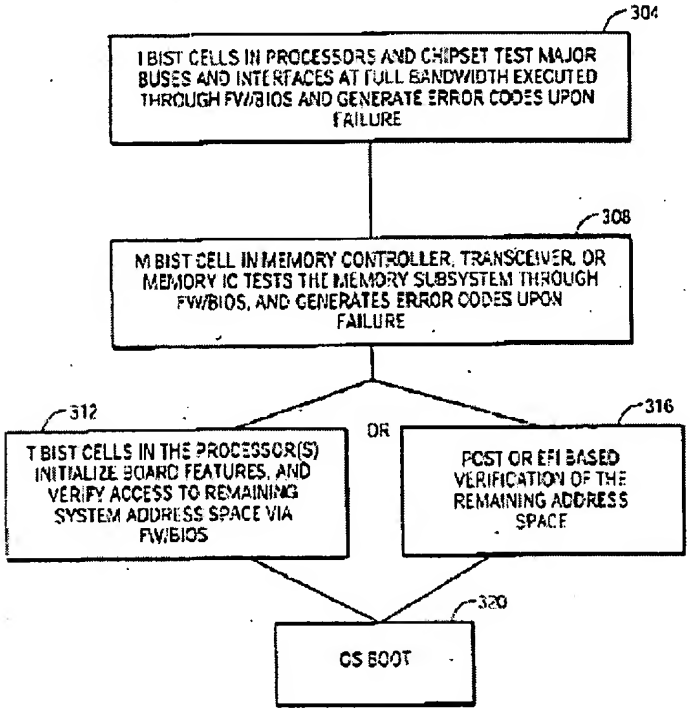


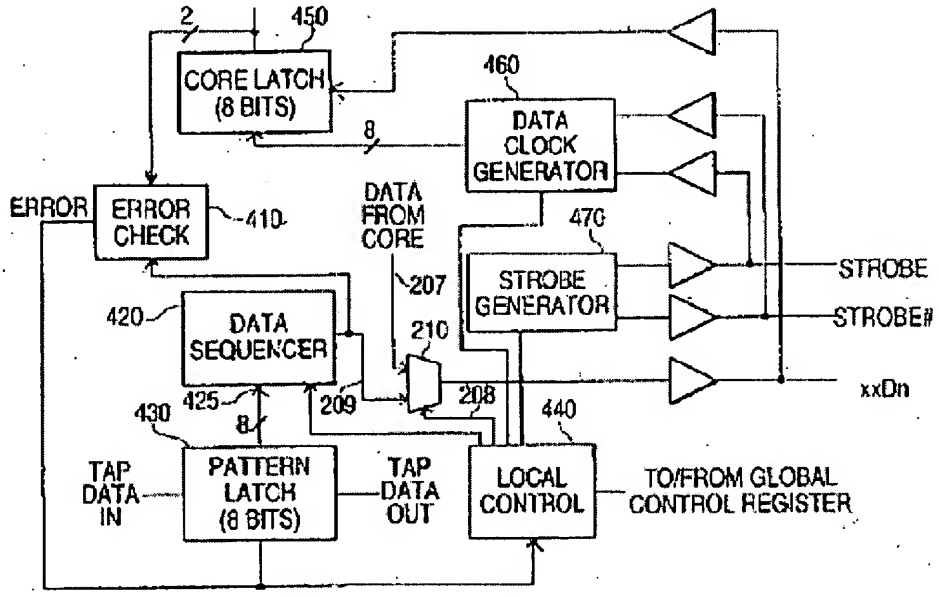
FIG. 3

Regarding claim 9:

Nejedlo discloses a system of integrated circuit (IC) devices, comprising: a carrier substrate (abstract, fig. 2, unit 224, 232); a host IC device having memory controller logic and being installed on the substrate (fig. 2, unit 224), the host IC device having built-in self test (BIST) generator logic coupled between a plurality of driver circuits and the memory controller logic (fig. 2, unit224, 232, 266), to a) transmit, at speed, address and command information generated by the controller logic, using the plurality of driver circuits in a normal mode of

operation for the IC device (page 1, section 0014) and b) transmit, at speed, test symbols (fig. 5, unit 608, 610, 606), using the plurality of driver circuits in a test mode of operation for the IC device during which an interconnect between the IC device and another device is tested (fig. 2, unit 224, 232, 228),

FIG. 4

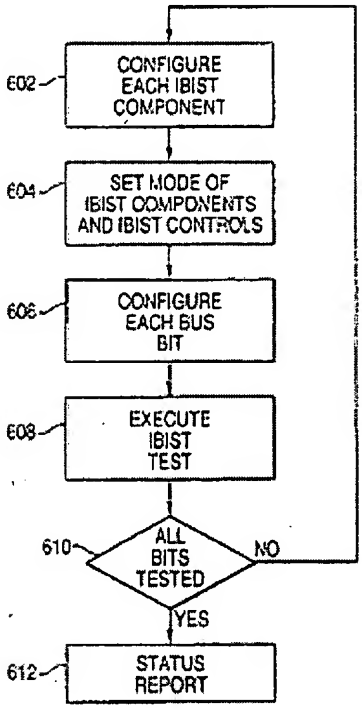


the host IC device having BIST checker logic coupled between a plurality of receiver circuits and the memory controller logic (fig. 2, unit 224, 228, 232), to a) forward data, received by the plurality of receiver circuits, to the memory controller logic in said normal mode of operation for the IC device (page 1, section 0014) and b) determine error in test symbols (fig. 4, unit 410) received by the plurality of receiver circuits in a test mode of operation for the IC device during which an interconnect between the IC device and another device is tested

(fig. 5, unit 612); and a first main memory module being installed on the substrate to communicate with the host IC device (fig. 2, unit 224,228), the first module having a memory buffer circuit with repeater capability to a) forward address and command information from the memory controller logic to a second main memory module (fig. 2, unit 224, 228,232), and b) forward read data from the second main memory module to the memory controller logic (fig. 2, unit 232, 228), the first module having first BIST checker logic to determine error in the test symbols transmitted by the BIST generator logic of the host IC device (fig. 4, unit 410, 420).

Regarding claim 6, Nejedlo further discloses using of DRAM in the test (page 2, section 0019); Regarding claim 7, Nejedlo further discloses a plurality of third and fourth signal connection points being installed on the substrate (fig. 2, unit 224, 228, 232); and wherein the buffer device includes a further plurality of driver circuits whose outputs are coupled to the plurality of third signal connection points (fig. 2, unit 266), respectively, and further logic to a) forward address and command information, that has been received from outside the module (fig. 3, unit 312, 316), at speed using the further plurality of driver circuits (fig. 4, unit 460) and b) determine error in test symbols, that have been received from outside the module at speed via the plurality of fourth signal connection points, in a test mode of operation module (fig. 4, unit 410);

FIG. 5



Regarding claim 8, Nejedlo further discloses to decode local memory command, address and data and send to plurality of memory devices (fig. 3, unit 312, 316); Regarding claim 10, Nejedlo further discloses the second main memory module installed on the substrate to communicate with the host IC device through the first main memory module (fig. 2, unit 224), the second module to re-transmit the test symbols transmitted by the host IC device and forwarded by the first module, back to the first module (fig. 2, unit 228); Regarding claim 11, Nejedlo further discloses second BIST checker logic to determine error in the re-transmitted test symbols received from the second module (fig. 2, unit 266, fig. 4, unit 410); Regarding claim 12, Nejedlo further discloses processor main memory to access

memory (fig. 2, unit 232); Regarding claim 13, Nejedlo further discloses system chipset for peripherals (fig. 2, unit 250).

Response to Arguments

3. Applicant's arguments filed 10/11/2005 have been fully considered but they are not persuasive.

The applicant seems to argue inherent issues of the 'missing element' of the prior art. Reminds to the applicant that to anticipate a claim, the reference must teach every element of the claim, A claim is anticipated only if each and every elements as set forth in the claim is found, either expressly or inherently, in a single prior art reference, See Verdegaal Bros. V. union Oil Co. of California, 814F2d 628,631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The arguments of counsel cannot take the place of evidence in the record. In re Schulze, 346 F.2d 600, 602, 145 USPQ 716, 718 (CCPA 1965), In re Geisler, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997).

A. Applicant argues in the arguments that the prior art does not show every elements of claim 5, please refer to the above rejection regarding claim 5.
The fact that Nejedlo discloses a BIST system, one of ordinary skill in the art at the time the invention was made know that BIST contains all self sustaining circuitry to support the prócessor (including core (The pc bible page 20, 31, 143), memory decoder (The pc bible page 31), address decoder (The pc bible page 901), memory buffer (The pc bible page 30, specially for Intel CPU core) (that's why they call it BIST) which is fabricate on a semiconductor wafer as the

applicant name it 'carrier substrate' system as show Nejedlo disclosure in page 1-2, section 0002-0021, fig. 2, unit 224, 228, fig. 1, unit 108, IC and semiconductor devices, page 76, 77, 78.

B. Applicant continues to argue in the arguments that the prior art does not show ' plurality of driver circuits whose outputs are coupled to the plurality of first signal connection points, respectively, and logic to a) forward read data, provided by the memory devices, at speed using first plurality of drivers in a normal mode of operation for the module, and b) determine error in test symbols received from outside the module at speed using the plurality of second connection points in a test mode of operation for the module during which a chip-to-chip connection between the module and another device is tested'. The applicant recited the basic/inherent function of cpu/processor core on page 1, section 108 and PCI bus function of the fig. 2, unit 254 and IO system communication in fig. 2, unit 254 which Nejedlo disclosure in his invention.

C. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung S Lau whose telephone number is 571-272-2274. The examiner can normally be reached on M-F 9-5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 571-272-2269. The fax phone numbers for the organization where this application or proceeding is assigned is 703-872-9306 Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TL

MICHAEL NGHIEM
PRIMARY EXAMINER